



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,046	08/28/2003	Toru Takayama	0756-7193	7230
31780	7590	01/04/2008		
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			EXAMINER NGUYEN, THANH T	
			ART UNIT	PAPER NUMBER
			2813	
			MAIL DATE	DELIVERY MODE
			01/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/650,046	Applicant(s) TAKAYAMA ET AL.	
	Examiner Thanh T. Nguyen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3, 5, 8, 13, 18, 23, 28, 33, 36-43, 45, 47-57, 74-80 and 82-87 is/are pending in the application.
- 4a) Of the above claim(s) none is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3, 5, 8, 13, 18, 23, 28, 33, 36-43, 45, 47-57, 74-80 and 82-87 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/24/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/24/07 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 82-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka (U.S. Patent Publication No. 2007/0087492).

Referring to figures 34-36, Yamanaka teaches a manufacturing method for a semiconductor device, comprising:

Heating an entire surface of a substrate by radiation heating from a first heat source (see paragraph# 458, figure 34(2));

Forming semiconductor layer (67) on the substrate (61);

Forming an insulating layer (68) over the semiconductor layer (67) includes a region to become at least a channel region of the thin film transistor (see paragraph# 462, figure 35(7));

Forming a conductive layer (75) over the semiconductor layer (67) with insulating layer (68) interposed between (see figure 35(5));

Selectively heating the semiconductor layer (67) by using a second heat source capable of radiating an electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band (see paragraph# 471, it is noted that UV light band is within the visible light band (400-800nm).). It is inherent that heating substrate which include every single layer on/in the substrate will be heated as well (the conductive layer, the semiconductor layers and the insulating layer...etc.).

Regarding to claim 83, the selective heating of the semiconductor layer is performed by using the second heat source capable of radiating an incoherent electromagnetic wave (see paragraph# 471).

Regarding to claim 38, 39, 84, substrate is a glass substrate (see paragraph# 170).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 5, 8, 13, 28, 33, 74, 76-77, 79-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al. (U.S. Patent Publication No. 2002/0056839) in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Referring to figures 1-9f, Joo et al. teaches a manufacturing method for a semiconductor device comprising:

Forming at least first and second semiconductor layers (33, amorphous silicon) that are divided from each other in an island-like shape over a substrate surface having an insulating surface (32, silicon oxide, see figures 3a), wherein each of the first and second semiconductor layers includes a region to become at least a channel region of a thin film transistor (see paragraph# 26, figure 3a);

Forming a conductive layer (35, doped polysilicon) covering an entire surface of each of the first and second semiconductor layers (33) with an insulating layer (34) interposed the between (see figure 3b, paragraph# 28); and

Etching conductive layer to form at least first and second gate electrodes (35) over the first and second semiconductor layers, respectively (see figures 3b-3c, paragraph# 28-29)

Selectively heating the first and second semiconductor layer by irradiating an incoherent electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band to thereby conducting heat treatment on the first and second semiconductor layers and the insulating layer, wherein the conductive layer extends beyond each periphery of the first and second semiconductor layers at least when the selected heating of the first and second semiconductor layers is performed (see paragraphs# 32, figure 3f). It is inherent that heating the conductive layer, the semiconductor layers and the insulating layer will also be heated.

Regarding to claims 8, 76, substrate is a glass substrate (see paragraph# 23).

Regarding to claims 13, 77, the substrate is quartz or sapphire (see paragraph# 23).

Regarding to claims 28, 79, forming a second conductive layer (36, nickel, see paragraph# 29) on the conductive layer (35) and forming a part of a gate electrode (35) using the conductive layer (35, see figures 3c-3d(1)).

Regarding to claim 74, a manufacturing method for a semiconductor device comprising:

Forming a semiconductor layer (33, amorphous silicon) over a substrate (30);

Forming an insulating layer (34, silicon oxide) over the semiconductor layer (33);

Forming a conductive layer (35) over the semiconductor layer with the insulating layer (34) interposed there between;

Selectively heating the semiconductor layer by using a heat source capable of radiating an incoherent electromagnetic wave within a wavelength band ranging at least a visible light band to an infrared band (see paragraphs# 32, figure 3f). It is inherent that heating the conductive layer, the semiconductor layers and the insulating layer will also be heated.

However, the reference does not teach the conductive films extends beyond each periphery of the first and second semiconductive layer when the heating of the first and second semiconductive layers is performed, the time range, and temperature range.

Yamazaki et al. teaches the conductive films extends beyond each periphery of the first and second semiconductive layer when the heating of the first and second semiconductive layers is performed (see paragraphs# 254, 294, meeting claims 3, 74. It is inherent that heating the conductive layer, the semiconductive layer and the insulating layer will also heated), the incoherent electromagnetic wave is irradiated for 30-300 seconds (see paragraph# 254, meeting claim 5), the heat treatment is performed at a temperature not less than a distortion point of the substrate (see paragraph# 254, 294, heating at the temperature 700-1000°C which is greater than 700°C (at the distortion point), meeting claims 33, 80).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form plurality of semiconductive island, etching the conductive layer after the selective heating for 30-300 second at the temperature greater than distortion point of the substrate in process of Joo et al. as taught by Yamazaki et al. because forming plurality of semiconductor island would provide plurality of thin film transistors, etching the conductive layer to form the gate electrode, heating to crystallized the layer as well as to activate the impurity added to the film.

Claims 18, 23, 75, 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joo et al. (U.S. Patent Publication No. 2002/0056839) in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1) as applied to claims 3, 5, 8, 13, 28, 33, 74, 76-77, 79-80 above in view of Yamazaki et al. (U.S. Patent Publication No. 2002/0000551).

Joo et al. in view of Yamazaki et al. teaches a method of forming a semiconductor device. However, Yamazaki does not teach the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, forming a first conducting film comprising metal nitride and forming a second conducting film over the first conducting film as a part of the gate electrode.

Regarding to claims 23, 78, the conductive film comprises metal nitride (see paragraph# 245).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form a quartz substrate in process of Joo et al. as taught by Yamazaki et al. in order for light transparent or to form an insulating substrate, forming the conductive film on the gate insulating film in order to form gate electrode for TFT device.

Regarding to claims 18, 75, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e. - a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band in process of Joo et al. in order to optimize the process.

Claims 36-41, 45, 47-53, 85-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka (U.S. Patent Publication No. 2007/0087492) as applied to claims 82-84 above in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Referring to figures 34-36, Yamanaka teaches a manufacturing method for a semiconductor device, comprising:

Heating an entire surface of a substrate by radiation heating from a first heat source (see paragraph# 458, figure 34(2));

Forming semiconductor layer (67) on the substrate (61);

Forming an insulating layer (68) over the semiconductor layer (67) includes a region to become at least a channel region of the thin film transistor (see paragraph# 462, figure 35(7));

Forming a conductive layer (75) over the semiconductor layer (67) with insulating layer (68) interposed between (see figure 35(5));

Selectively heating the semiconductor layer (67) by using a second heat source capable of radiating an electromagnetic wave within a wavelength band ranging at least from a visible light band to an infrared band (see paragraph# 471, it is noted that UV light band is within the visible light band (400-800nm).). It is inherent that heating substrate which include every single layer on/in the substrate will be heated as well (the conductive layer, the semiconductor layers and the insulating layer...etc.).

Regarding to claim 83, the selective heating of the semiconductor layer is performed by using the second heat source capable of radiating an incoherent electromagnetic wave (see paragraph# 471).

Regarding to claim 38, 39, 84, substrate is a glass substrate (see paragraph# 170).

Regarding to claim 40, 41, substrate is selected from one of quartz and sapphire (see paragraph# 170).

Regarding to claim 45, the insulating layer (68) cover a top surface and a side surface of each of the semiconductor layers (67, see figure 34(4)).

Regarding to claim 47, the insulating layer includes a laminate of silicon oxide film and silicon nitride film (68, see figure 34(4), paragraph# 195).

However, the reference does not teach the conductive film can be form by using metal or metal nitride, or metal silicide and the conductive film having higher absorptance with respect to an incoherent electromagnetic wave within a wavelength band ranging from visible light band to infrared band than the substrate.

Yamazaki teaches in paragraph# 90, a method of forming a conductive film by using metal or metal nitride, or metal silicide (meeting claims 48-83, 85-87). Since the conductive film (non-transparent film) is a metal, metal nitride, or metal silicide which has a very high conductivity therefore it has higher absorptance with respect to an incoherent electromagnetic wave within a wavelength band ranging from visible light band to infrared band than the glass or ceramic substrate. As well as the same material would provide the same result of absorptance with respect to an incoherent electromagnetic wave (meeting claims 36-37).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a conductive film by using metal or metal nitride, or metal silicide in process of Yamanaka as taught by Yamazaki because the conductive film of metal or metal nitride, or metal silicide is known in the semiconductor art to high conductivity gate electrode.

Claims 42-43, 54-55, 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka (U.S. Patent Publication No. 2007/0087492) in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1) as applied to claims 36-41, 45, 47-53, 85-87 above further in view of Yamazaki et al. (U.S. Patent Publication No. 2001/0049163A1).

Yamanaka in view of Yamazaki et al. teaches a method of forming a TFT having a semiconductor layers, annealing the semiconductor layer, forming an insulating film on the semiconductor layer, forming a conductive film on the insulating film, and heating the semiconductor film.

However, the reference does not teach heating of the first and second semiconductive layers is performed at temperature range that not lower than a distortion point of the substrate, and substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band.

Yamazaki et al. teaches heating of the first and second semiconductive layers is performed (see paragraphs# 254, 294. It is inherent that heating the conductive layer, the semiconductive layer and the insulating layer will also heated), the heat treatment is performed at a temperature not less than a distortion point of the substrate (see paragraph# 254, 294, heating at the temperature 700-1000°C which is greater than 700°C (at the distortion point), meeting claims 56-57).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form plurality of semiconductive island, heating for 30-300 second at the temperature greater than distortion point of the substrate in process of Yamanaka as taught by Yamazaki et al. because heating process is known in the semiconductor art to crystallized the layer as well as to activate the impurity added to the film.

Regarding to claims 42-43, 54-55, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to form the substrate has a transmittance of 50 % or higher with respect to the electromagnetic wave within the wavelength band in process of Yamanaka in order to optimize the process in formation of TFT device.

Conclusion

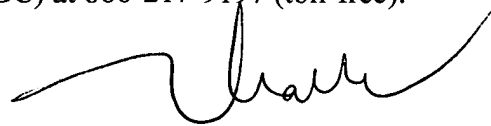
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Art Unit: 2813

applications is available through Private PAIR only. For more information about the PAIR system, see <http://pairdirect.uspto.gov>. Should you have questions on access to thy Private PAIR system, contact the Electronic Business center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thanh', with a long horizontal stroke extending to the left.

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN